UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,791	11/19/2003	Hiroaki Kubo	JP920020167US1	6146

7590   04/30/2007
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EXAMINER
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ART UNIT	PAPER NUMBER
2621	

MAIL DATE	DELIVERY MODE
04/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____ .

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-7_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-7_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _19 November 2003_ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☒ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _20031119, 20070301_ .

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____ .

DETAILED ACTION

Priority

1.   Acknowledgment is made of applicant's claim for foreign priority based on an

application filed in Japan on 26 November 2002. It is noted, however, that applicant

has not filed a certified copy of the 2002-342268 application as required by 35

U.S.C. 119(b).

Drawings

2.   Figure 11 should be designated by a legend such as --Prior Art-- because only

that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in

compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the examiner does not accept the changes, the

applicant will be notified and informed of any required corrective action in the next Office

action. The objection to the drawings will not be held in abeyance.

Specification

3.   The disclosure is objected to because of the following informalities: the last

paragraph of the specification (page 16) is incomplete.

        Appropriate correction is required.

Claim Rejections - 35 USC § 101

4.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5.   Claim 7 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. For a computer processing or software claim to be statutory, it must recite the essential term of "a computer-readable medium encoded with a computer program". This reflects a computer element that defines structural and functional interrelationships between the computer program and the rest of the computer and permits the computer program's functionality to be realized. See *In re Lowry*, F.3d at 1583-84, 32 USPQ2d at 1035. In the present invention, the term "program storage device" is not a defined technical phrase, and is not equivalent to "a computer readable medium".

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 1, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6233253 B1 (Settle et al.) in view of US Patent 6,297,794 B1

(Tsubouchi et al.), of which corresponding Japanese Patent Application Publication 10-116064 A was cited in the Information Disclosure Statement of 01 March 2007. Claims 1, 6, and 7 of the present invention are co-extensive in scope, with claim 1 as a hardware embodiment, claim 6 as a method, and claim 7 as a software embodiment. Settle et al. teaches a format conversion system that multiplexes video data from multiple sources into one data format for transmission (abstract). Regarding the "header generation device" of apparatus claim 1, packetizers 18 in Settle et al. add MPEG transport headers to the data from the video sources (column 4, lines 47-49). Regarding the step of "generating a packet header" in method claim 6, the packetizers perform formatting steps 214 and 245, which add packet headers to video data in the method shown in figure 1 of Settle et al. (column 3, lines 23-29, 50-52). Regarding the step of "generating a packet header" in software claim 7, the packetizing method may be implemented on a computer (column 4, lines 26-30). Signals from the different data sources are multiplexed to produce a constant output data rate (column 7, lines 28-30). Although clock references are periodically added to the multiplexed transport stream (column 5, lines 63-66), this information is used to synchronize audio and video data at a decoding step, not at encoding.

Settle et al. discloses a header-generating device, but not the storing of unpacketized video data in a memory, or detecting a synchronizing signal. Tsubouchi et al. teaches a system with a variety of video devices, including a video capture device (column 8, lines 17-25) and an MPEG encoder (column 6, lines 50-58), which share a dedicated bus for audio/video data. Each device includes an output buffer for outputting

data onto the bus (column 2, lines 55-57). This bus includes a ZV control line, on which

an enable signal can be transmitted. The control line may be daisy-chained to each

device (column 5, lines 27-36), or it may be common to all devices (column 10, line 13-

15). In one embodiment, a pulse generating circuit in each device sends out a pulse on

the control line to disable other devices and free up the A/V bus (column 11, lines 32-

58). This setup is pulse-width modulated, with each pulse generating circuit producing

a pulse of a different width (column 11, lines 10-32). Each device also includes a flip-

flop that stores the enable/disable state for the device. A particular device can only use

the video when its flip-flop is set to enable (column 10, lines 41-56). Then, until a pulse

from a different device is detected, resetting the flip-flop, a device may be free to output

video to the bus. The packetizers of Settle et al. generate MPEG transport stream

packets, which are known to have a specific packet header structure and payload length

corresponding to each packet header (column 4, lines 39-42). In Settle et al., the

repetition rate of a series of packets from each source is dependent on the bandwidth of

the multiplexer and transmitter, and the data rate of incoming video data.

Tsubouchi et al. teaches that it was known to store video in a buffer, and only

release video from the buffer in response to a synchronizing signal. Therefore, it would

have been obvious at the time of the invention was made to store video data into a

buffer and to detect a synchronizing signal as taught by Tsubouchi et al., since

Tsubouchi et al. states in column 2, lines 49-50 that such a modification would prevent

collision between video data from multiple sources.

8.   Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Settle et

al. in view of Tsubouchi et al. as applied to claim 1 above, and further in view of US

Patent 5,812,760 A (Mendenhall et al). Settle et al. in combination with Tsubouchi et al.

teach the claimed invention except for a counter that counts packet header size.

Mendenhall et al. teaches a video data parser that manages data bytes with status flags

(abstract). Regarding claim 2, in an MPEG-2 mode of operation, when a packet layer is

identified, a packet header counter and packet length counter are loaded (column 10,

lines 3-6). As data is streamed bytewise from FIFO memory 224 via header buffer 272,

packet header counter 260 decrements until the counter reaches one, at which point the

last byte in the packet header is loaded (column 10, lines 9-12). Then, multiplexer 285

switches to packet data buffer 280, and packet length counter 266 is decremented until

the last data byte is processed, when the counter reaches one (column 10, lines 12-16).

The parser responds to sync flag 230, which is raised when a start code is detected

(column 5, lines 27-32), and processes data until the sync flag is reset.

Mendenhall et al. teaches that it was known to count the length of an MPEG-2

packet header and a packet. Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to count packet header length

as taught by Mendenhall et al., since Mendenhall et al. states in column 9, lines 52-55

and column 10, lines 1-3 that such a modification would allow a system to handle a

video stream with customizable packet lengths.

9.   Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Settle et al., Tsubouchi et al., and Mendenhall et al. as applied to claim 2 above, and

further in view of US Patent 5,671,260 A (Yamauchi et al.). Although claim 3 is

independent, it discloses a narrower version of every limitation in claims 1 and 2.

However, the limitation of claim 3 that the "synchronizing signal" in claim 2 is a

"horizontal synchronizing signal for the video data" places the scope of claim 3 outside

of the combination of Settle et al. and Tsubouchi et al. Claim 3 additionally specifies

that the output video data is in the same packet format as an MPEG-2 Transport Stream

packet, and that the memory for storing video data is a FIFO memory. Regarding the

FIFO memory, video capture 31 of Tsubouchi et al. contains an output buffer for

outputting video to a dedicated bus (column 2, lines 55-57). Alternatively, data in

Mendenhall et al. is explicitly stored in FIFO 224, where data bytes are locked with a

sync flag (column 4, lines 3-11). Regarding the MPEG-2 Transport Stream packet,

Settle et al. formats video to a format compatible with MPEG transport packets (column

4, lines 39-42). However, the synchronization pulse in Tsubouchi et al. or the sync flag

in Mendenhall et al. is not a horizontal synchronization signal.

        Yamauchi et al. teaches a digital signal processing apparatus that includes a

Phase Locked Loop (PLL) that produces a clock signal locked to the horizontal

synchronization signal included with the video input (abstract). Synchronization signal 2

extracts an HSYNC and VSYNC signal from input video signal Sv (column 4, lines 44-

50), and control signal generator 12 extracts the HYSNC signal to produce reference

signal Sf1 (column 2, lines 51-56). PLL 13 generates a clock signal Sc1 from reference

signal Sf1 (column 4, lines 61-63), and A/D converter 5 samples video signal Sv with

respect to the clock signal Sc1, producing digital video Svc (column 5, lines 27-32).

Digital video Svc is stored into memory 6 based on write signal Sw, which is based on

the HSYNC and VSYNC signals from the original video (column 5, lines 24-26). Then,

the video memory is only written to when video data is transmitted in signal Sv, such as

columns 123-824 in a given line in the NTSC standard (column 5, lines 19-24).

The references cited in section 8 *supra* disclose the claimed invention except for

digitizing video according to a horizontal synchronization signal. Yamauchi et al.

teaches that it was known to sample video based on a horizontal synchronization signal,

as set forth in column 5, lines 6-39. Therefore, it would have been obvious to one

having ordinary skill in the art at the time the invention was made to synchronize a video

transcoder to HSYNC as taught by Yamauchi et al. because Yamauchi states in column

8, lines 1-4 that such a modification would ensure that only relevant video data is

encoded and not non-video data transmitted in a horizontal blanking interval, regardless

of the variability of this interval.

Regarding the "data valid signal" of claim 4, in Yamauchi et al., video memory

write signal Sw is only enabled during the period in a particular line in a video when

converted video signal Svc corresponds to effective video data (column 5, lines 17-26).

Then, only valid video data is transmitted. Regarding the memory reset in claim 5, for

each given line in an NTSC format, writing signal Sw controls a memory to not read

data for the first 122 cycles of clock Sc1 produced from the horizontal synchronization

signal, then to write data for the next 720 clock cycles, and to release data for the last

16 clock cycles (column 8, lines 1-15). Yamauchi discloses the claimed invention

except for producing a data valid signal based on a horizontal synchronization signal

from a memory write controller instead of a packet header length counter. However, the

"data valid signal" in claims 4 and 5 is considered equivalent under the Doctrine of

Equivalents to the "writing signal" in Yamauchi et al, since in both the present invention

and in Yamauchi et al., the signal performs the same function (controlling a memory

storing a video signal), in substantially the same way (in response to a horizontal

synchronization signal), to produce substantially the same result (outputting only valid

data not in the horizontal blanking interval). See *Graver Tank & Mfg. Co. v. Linde Air

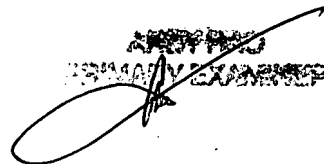Products*, 339 U.S. 605, 85 USPQ 328 (1950).

Conclusion

10.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. US Patent 4,237,553 (Larsen) discloses a ring network in which

each station in the network includes a counter that counts bits in a packet header. US

Patent 6,553,147 B2 (Chai et al.) discloses an MPEG transport stream encoder and

decoder with resynchronization markers. US Patent Application 7,027,515 B2 (Lin) and

US Patent Application Publication 2003/0031261 A1 (Valente et al.) each disclose an

MPEG decoder that uses resynchronization markers for error concealment. US Patent

Application Publication 2002/0085632 A1 (Choi et al.) discloses a transmitter that

inserts MPEG packet headers into supplemental data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David N. Werner whose telephone number is (571) 272-9662. The examiner can normally be reached on Monday-Friday from 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571) 272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DNW